Product data sheet



1. General description

The 74ABT125 is a quad buffer/line driver with 3-state outputs controlled by the output enable inputs (nOE). A HIGH on nOE causes the outputs to assume a high impedance OFF-state. This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

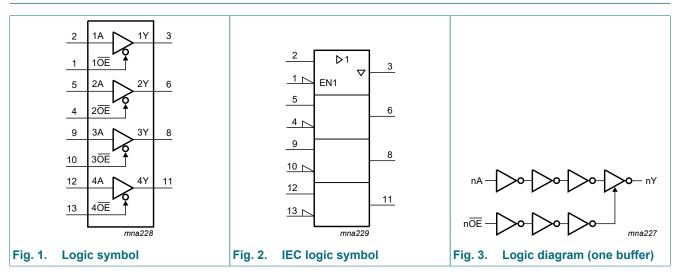
- Supply voltage range from 4.5 V to 5.5 V
- · BiCMOS high speed and output drive
- Direct interface with TTL levels
- Power-up 3-state
- Inputs are disabled during 3-state mode
- IOFF circuitry provides partial Power-down mode operation
- Latch-up protection exceeds 500 mA per JESD78B class II level A
- Quad bus interface
- 3-state buffers
- Live insertion and extraction permitted
- Output capability: HIGH -32 mA; LOW +64 mA
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C

3. Ordering information

Type number	Package	Package							
	Temperature range	Name	Description	Version					
74ABT125D	-40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	<u>SOT108-1</u>					
74ABT125PW	-40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	<u>SOT402-1</u>					
74ABT125BQ	-40 °C to +85 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	<u>SOT762-1</u>					

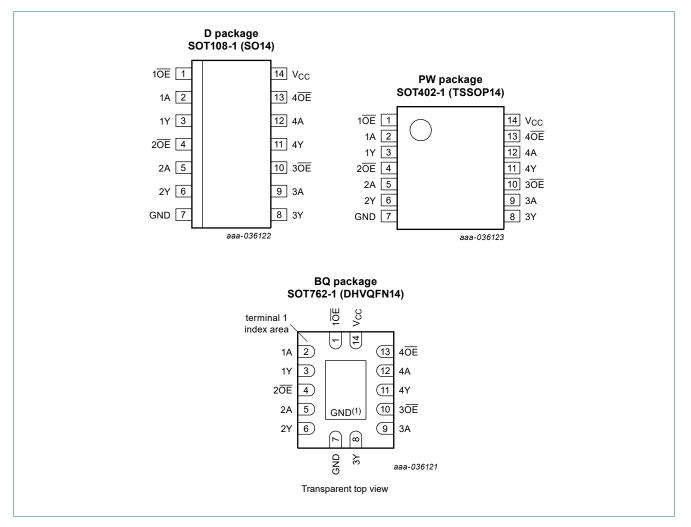
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4. Functional diagram



5. Pinning information

5.1. Pinning



(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

5.2. Pin description

Table 2. Pin description						
Symbol	Pin	Description				
10E, 20E, 30E, 40E	1, 4, 10, 13	output enable input (active LOW)				
1A, 2A, 3A, 4A	2, 5, 9, 12	data input				
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	data output				
GND	7	ground (0 V)				
V _{CC}	14	supply voltage				

6. Functional description

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Inputs	Output	
nŌE	nA	nY
L	L	L
L	Н	Н
Н	x	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC}	supply voltage			-0.5	+7.0	V
VI	input voltage		[1]	-1.2	+7.0	V
Vo	output voltage	output in OFF-state or HIGH-state	[1]	-0.5	+5.5	V
I _{IK}	input clamping current	V ₁ < 0 V		-18	-	mA
I _{OK}	output clamping current	V _O < 0 V		-50	-	mA
I _O	output current	output in LOW-state		-	128	mA
Tj	junction temperature		[2]	-	150	°C
T _{stg}	storage temperature			-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +85 °C	[3]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

[3] For SOT108-1 (SO14) package: Ptot derates linearly with 10.1 mW/K above 100 °C.

For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C. For SOT762-1 (DHVQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

8. Recommended operating conditions

Table 5. Operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Мах	Unit
V _{CC}	supply voltage		4.5	5.5	V
VI	input voltage		0	V _{CC}	V
V _{IH}	HIGH-level input voltage		2.0	-	V
V _{IL}	LOW-level Input voltage		-	0.8	V
I _{OH}	HIGH-level output current		-32	-	mA
I _{OL}			-	64	mA
Δt/ΔV	input transition rise and fall rate		-	10	ns/V
T _{amb}	ambient temperature	in free air	-40	+85	°C

9. Static characteristics

Symbol	Parameter	Conditions			25 °C		-40 °C t	o +85 °C	Unit
				Min Typ		Max	Min Max		
V _{IK}	input clamping voltage	V _{CC} = 4.5 V; I _{IK} = -18 mA		-	-0.9	-1.2	-	-1.2	V
V _{OH}	HIGH-level output	$V_{I} = V_{IL} \text{ or } V_{IH}$							
	voltage	V _{CC} = 4.5 V; I _{OH} = -3 mA		2.5	2.9	-	2.5	-	V
		V _{CC} = 5.0 V; I _{OH} = -3 mA		3.0	3.4	-	3.0	-	V
		V _{CC} = 4.5 V; I _{OH} = -32 mA		2.0	2.4	-	2.0	-	V
V _{OL}	LOW-level output voltage	$V_{\rm CC}$ = 4.5 V; I _{OL} = 64 mA; $V_{\rm I}$ = V _{IL} or V _{IH}		-	0.35	0.55	-	0.55	V
l _l	input leakage current	V _{CC} = 5.5 V; V _I = GND or 5.5 V		-	±0.01	±1.0	-	±1.0	μA
I _{OFF}	power-off leakage current	$V_{CC} = 0.0 \text{ V}; \text{ V}_{\text{I}} \text{ or } \text{V}_{\text{O}} \le 4.5 \text{ V}$		-	±5.0	±100	-	±100	μA
I _{O(pu/pd)}	power-up/power-down output current	V_{CC} = 2.1 V; V_O = 0.5 V; V_I = GND or V_{CC} ; \overline{OE} = don't care	[1]	-	±5.0	±50	-	±50	μA
l _{oz}	OFF-state output	V_{CC} = 5.5 V; V_{I} = V_{IL} or V_{IH}							
	current	V _O = 2.7 V		-	1.0	50	-	50	μA
		V _O = 0.5 V		-	-1.0	-50	-	-50	μA
I _{CEX}	output high leakage current	HIGH-state; $V_0 = 5.5 V$; $V_{CC} = 5.5 V$; $V_I = GND$ or V_{CC}		-	5.0	50	-	50	μA
lo	output current	V_{CC} = 5.5 V; V_{O} = 2.5 V	[2]	-50	-100	-180	-50	-180	mA
I _{CC}	supply current	V_{CC} = 5.5 V; V_{I} = GND or V_{CC}							
		outputs HIGH-state		-	65	250	-	250	μA
		outputs LOW-state		-	12	15	-	30	mA
		outputs disabled		-	65	250	-	250	μA

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Symbol	Parameter	ter Conditions		25 °C			-40 °C to +85 °C		
			Min	Тур	Max	Min	Мах	1	
ΔI _{CC}	additional supply current	ber control pin; $V_{CC} = 5.5 V$; [3] one control input at 3.4 V, other inputs at V_{CC} or GND							
		outputs enabled	-	0.5	1.5	-	1.5	mA	
		outputs disabled	-	50	250	-	250	mA	
		one enable input at 3.4 V and other inputs at V _{CC} or GND; outputs disabled	-	0.5	1.5	-	1.5	mA	
CI	input capacitance	$V_{I} = 0 V \text{ or } V_{CC}$	-	4	-	-	-	pF	
Co	output capacitance	outputs disabled; $V_0 = 0 V$ or V_{CC}	-	7	-	-	-	pF	

[1] This parameter is valid for any V_{CC} between 0 V and 2.1 V, with a transition time of up to 10 ms.

From V_{CC} = 2.1 V to V_{CC} = 5 V \pm 10 %, a transition time of up to 100 μ s is permitted.

[2] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[3] This is the increase in supply current for each input at 3.4 V.

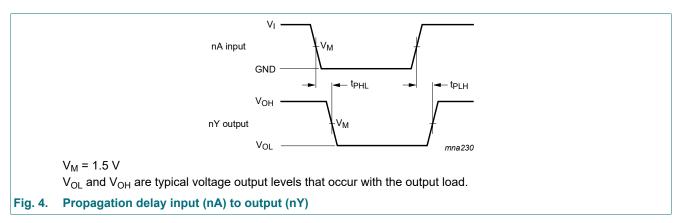
10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V. Test circuit is shown in Fig. 6.

Symbol	Parameter	Conditions	25 °C; V _{CC} = 5.0 V			-40 °C to V _{CC} = 5.0	Unit	
			Min	Тур	Мах	Min	Мах	
t _{PLH}	LOW to HIGH propagation delay	nA to nY, see <u>Fig. 4</u>	1.0	2.8	4.1	1.0	4.6	ns
t _{PHL}	HIGH to LOW propagation delay	nA to nY; see <u>Fig. 4</u>	1.0	3.1	4.6	1.0	4.9	ns
t _{PZH}	OFF-state to HIGH propagation delay	nOE to nY; see <u>Fig. 5</u>	1.0	3.2	5.0	1.0	5.9	ns
t _{PZL}	OFF-state to LOW propagation delay	nOE to nY; see <u>Fig. 5</u>	1.0	4.2	6.2	1.0	6.8	ns
t _{PHZ}	HIGH to OFF-state propagation delay	nOE to nY; see <u>Fig. 5</u>	1.0	4.1	5.4	1.0	6.2	ns
t _{PLZ}	LOW to OFF-state propagation delay	nOE to nY; see <u>Fig. 5</u>	1.5	2.8	5.0	1.5	5.5	ns

10.1. Waveforms and test circuit

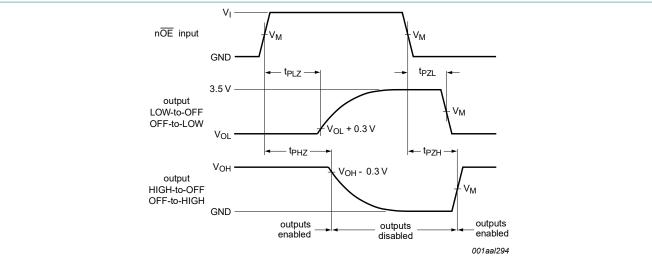


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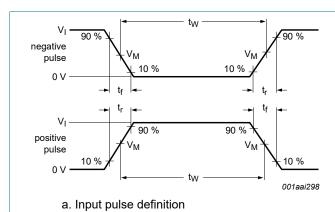
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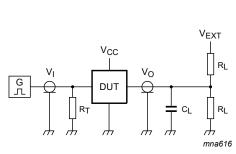


V_M = 1.5 V

 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 5. Enable and disable times







Test data is given in Table 8.

Test circuit definitions:

R_L = Load resistance.

 C_L = Load capacitance including jig and probe capacitance.

 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

Fig. 6. Test circuit for measuring switching times

Table 8. Test data

Input			Load		V _{EXT}			
VI	f _l	t _w	t _r , t _f	CL	RL	t _{PHL} , t _{PLH}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}
3.0 V	1 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	open	open	7.0 V

11. Package outline

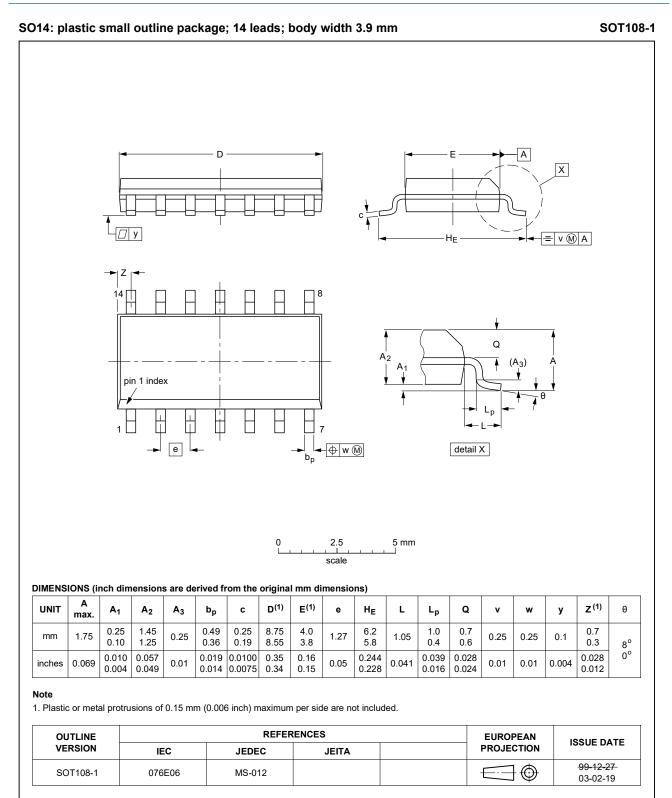


Fig. 7. Package outline SOT108-1 (SO14)

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Quad buffer; 3-state

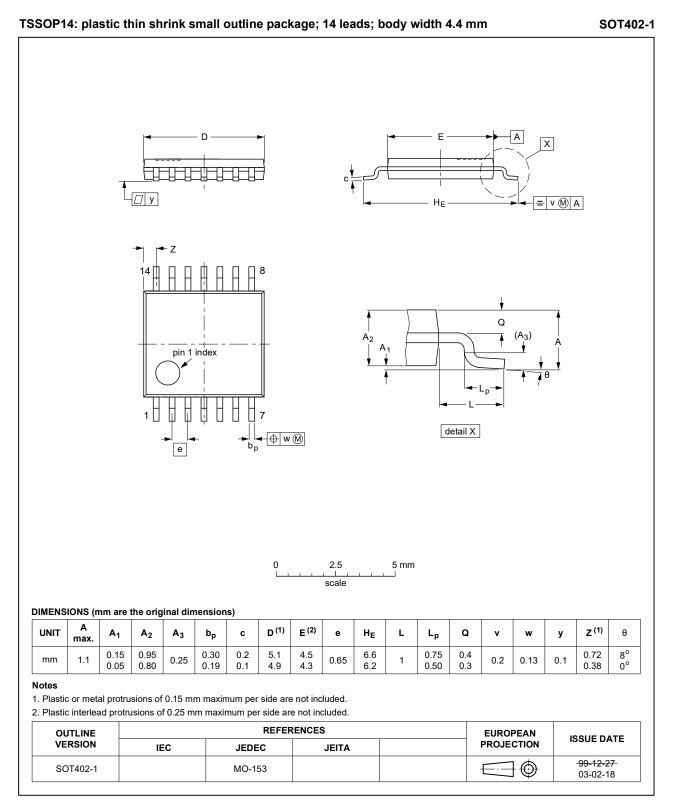


Fig. 8. Package outline SOT402-1 (TSSOP14)

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Quad buffer; 3-state

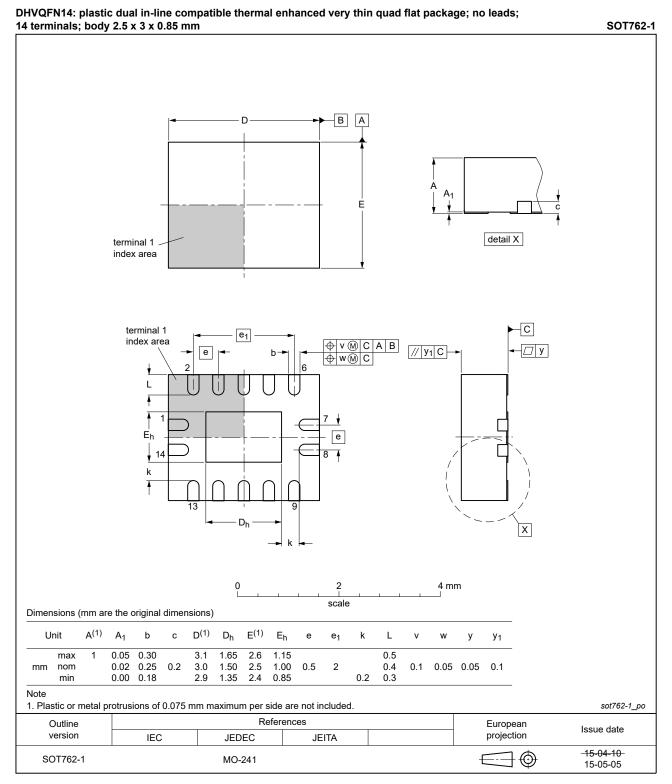


Fig. 9. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
ММ	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 10. Revision h		D. (
Document ID	Release date	Data sheet status	Change notice	Supersedes		
74ABT125 v.9	20230313	Product data sheet	-	74ABT125 v.8		
Modifications:	• <u>Table 6</u> : I _{CC(r}	_{nax)} value at +85 °C (outputs d	isabled) corrected. (errata).		
74ABT125 v.8	20210630	Product data sheet	-	74ABT125 v.7		
Modifications:	Nexperia. • Legal texts h • Type numbe • <u>Section 1</u> an	· · · · · · · · · · · · · · · · · · ·				
74ABT125 v.7	20151125	Product data sheet	-	74ABT125 v.6		
Modifications:	Type numbe	r 74ABT125N (SOT27-1) remo	ved.			
74ABT125 v.6	20111103	Product data sheet	-	74ABT125 v.5		
Modifications:	Legal pages	updated		-		
74ABT125 v.5	20101124	Product data sheet	-	74ABT125 v.4		
74ABT125 v.4	20100427	Product data sheet	-	74ABT125 v.3		
74ABT125 v.3	20080429	Product data sheet	-	74ABT125 v.2		
74ABT125 v.2	19980116	Product specification	-	74ABT125 v.1		
74ABT125 v.1	19960305	-	-	-		

Quad buffer; 3-state

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

 Please consult the most recently issued document before initiating or completing a design.

- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <u>https://www.nexperia.com</u>.

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